Daniel Leeds, 6.004 R12, March 24, 2006; Lecture and Tutorial Problems Excerpts
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## von Neumann Computer

Key idea: Memory holds not only data, but coded instructions that make up a program INSTRUCTIONS coded as binary data
PROGRAM COUNTER or PC:
Address of next instruction to be executed
logic to translate instructions into control signal for path



Fetch/Execute loop:
Fetch Mem[PC]
$\mathrm{PC}=\mathrm{PC}+4$
Execute fetched instruction
Repeat

Binary layout of the two Beta instruction formats:

| OPCODE | $\mathrm{r}_{\mathrm{c}}$ | $\mathrm{r}_{\mathrm{a}}$ | $\mathrm{r}_{\mathrm{b}}$ | unused |
| :--- | :--- | :--- | :--- | :--- |


| OPCODE | $r_{c}$ | $r_{a}$ | 16-bit signed constant |
| :--- | :--- | :--- | :--- |

Types of Beta assembly instructions:
Register Arithmetic: $\operatorname{ADD}(\mathrm{R} 1, \mathrm{R} 2, \mathrm{R} 3)$

$$
\begin{aligned}
& \mathrm{R} 3=\mathrm{R} 1+\mathrm{R} 2 \\
& \mathrm{Mem}[\mathrm{R} 2+\mathrm{c}]=\mathrm{R} 1 \\
& \mathrm{R} 3=1 \text { if } \mathrm{R} 1<\mathrm{R} 2 ; 0 \text { o.w. } \\
& \mathrm{R} 3=\mathrm{PC}+4 \\
& \mathrm{PC}=\mathrm{PC}+4+4 * 0 \times 20 \text { if } \mathrm{R} 2 ; \\
& \mathrm{PC}=\mathrm{PC}+4 \text { o.w. }
\end{aligned}
$$

Memory Access: $\quad \mathrm{LD}(\mathrm{R} 1, \mathrm{c}, \mathrm{R} 2)$
Compares: CMPLT(R1,R2,R3)
Branch:
BEQ(R1, 0x20, R2)

## More on memory:

$\mathrm{LD}(\mathrm{Ra}$, literal, Rc$)$ : "load value at address $R a+$ literal into register $R c$ "
$\mathrm{ST}(\mathrm{Rc}$, literal, Ra$)$ : "store value in register $R c$ into address literal $+R a$ "

```
    . = 0x100
ans: long(0)
    LD(R31, ans, R0)
```

ans $=0 \times 100$
$\mathrm{R} 0=0$ (the value at address $0 \times 100$ )

Programmable Machines
Problem 1
$F N=0 \quad A-B$ $\mathrm{FN}=1 \quad \mathrm{~B}-\mathrm{A}$


F Build a controller that will cause the circuit above to execute the following algorithm:

```
while (a != b)
    if (a > b) a = a - b;
```

    else \(\mathrm{b}=\mathrm{b}-\mathrm{a}\);
    |  | DRA | DRB | DRALU | LDA | LDB | FN |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Reg A <- A | 1 | 0 | 0 | 1 | 0 | X |
| Reg B <-B | 0 | 1 | 0 | 0 | 1 | X |
| A==B? |  |  |  |  |  |  |
| (if A>B) Reg A <- Reg A - Reg B |  |  |  |  |  |  |
| (else) Reg B <- Reg B - Reg A |  |  |  |  |  |  |
| (loop up to A=B?) |  |  |  |  |  |  |
| (if A==B) do nothing |  |  |  |  |  |  |

Machine Language:
Problem 4:
D Explain why PC-relative branch addressing is a good choice for computers like the Beta that can encode only a "small" constant in each instruction.

Problem 9: Which of the following Beta instruction sequences might have resulted from compiling the following C statement?

```
int x[20], y;
y = x[1] + 4;
A LD (R31,x+4,R0
    ST (R0, y+4,R31)
```

```
B CMOVE (4,RO)
```

B CMOVE (4,RO)
LD (R0,x,R1)
LD (R0,x,R1)
ST(R1,y,R0)

```
    ST(R1,y,R0)
```

C LD (R31, $x+4, R 0)$ ADDC (R0, 4, R0)
ST(R0,y,R31)

```
D ADDC (R31, \(\mathrm{x}+1, \mathrm{RO})\) ADDC (R0, 4, R0)
ST (R0,y,R31)
```

Problem 3: A Hand assemble the following:

```
I=0\times5678
B=0\times1234
LD(I,R0)
SHLC (R0, 2, R0)
LD (R0,B,R1)
MULC(R1, 17,R1)
ST(R1,B,R0)
```

Enjoy Spring Break!

